

PATENT

REMARKS

This paper is responsive to a non-final Office action dated January 30, 2004. Claims 9-36 were examined. Previously made rejections have been maintained and a new basis for rejection of claims 9-16 has been advanced. Applicant has amended the independent claims to overcome the rejections.

All claims have been rejected as anticipated under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,488,729 to Vegesna et al. (*Vegesna*). Applicant has previously identified discrepancies between *Vegesna* as actually disclosed and *Vegesna* as applied by the Office. One important discrepancy is that *Vegesna* performs (for a given instruction group) decode and scheduling so that the corresponding operations will be completed *within one CPU clock cycle, not over plural execution cycles*. The present application identifies certain pipeline advantages obtained by *completing for a particular instruction instance*, instruction grouping for dispatch *over plural execution cycles*.

Upon review of the outstanding Office action, it appears that the Examiner does not dispute the distinction as presented, but rather feels that it is possible to interpret the claim language in ways that skirt the distinction. Such was the state of affairs after the preceding action and the Examiner, acting for the Office in rejecting the present claims, has again discounted certain textual limitations thereof. As a result, the Office apparently interprets “performing X over plural cycles” as “performing X to completion in a single cycle only, but with regard to instructions that have been issued over plural prior cycles.” While Applicants are somewhat at a loss to understand how the Office would sustain this interpretation of the claims, we need not understand. Instead, since the Examiner’s comments indicate that he clearly understands the intended scope, we have (in an effort to expedite prosecution) amended to recite that scope using the Examiner’s own recitation.

Claims 9, 17, 26, 31 and 35 have each been amended to recite, using the Examiner’s preferred recitation of Applicant’s intended scope, that the particular step, act, function, operation, computation, structure or means (as appropriate to the language of each particular claim) be performed to completion during a number of cycles, during period of time, through a number pipeline stages (or the like) that is greater than one (1). In addition, each of the

## PATENT

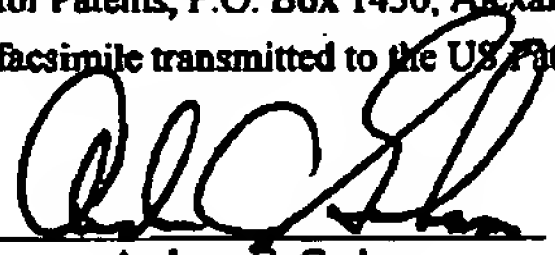
independent claims recites (in one way or another) that the relevant step, act, function, operation, computation, structure or means operates on a particular instruction instance or group of instructions being grouped for dispatch. Accordingly, Examiner proposal (in the prior action and maintained in the present action) that single-cycle instruction grouping and dependency checking for a first packet of instructions (i.e., in one single cycle) and later for a second (and unrelated) packet of instructions (i.e., in another single cycle) constituted performing relevant acts, *over plural execution cycles*, is not (or is no longer) sustainable.

Accordingly, all issues of unintended collateral scope envisioned by the Examiner have now been removed. All claims are allowable and a notice to that effect is respectfully requested.

For completeness and with regard to the Office's rejection of certain claims reciting evaluation or checking of non-deterministic conditions, Applicant notes that the Examiner's application of a definition of non-determinism is incorrect. In short, the Examiner concludes that a computation that produces one result based on a first set of input data, and that produces another result based on second set of input data, is non-deterministic. This is simply false. Building on the false premise, the Office reads inter-group dependency checking as a "non-deterministic" condition evaluation since such dependency check may identify that instruction groups are independent (a first result) or exhibit a dependency (a second result). Based on the faulty analysis, the Office proceeds reject various claims. While the affected claims (at least claims 30 and 31) are each allowable for the separate reasons presented above, Applicant wishes to make the record clear that it is not acquiescing in the incorrect application of a definition or the resulting faulty analysis.

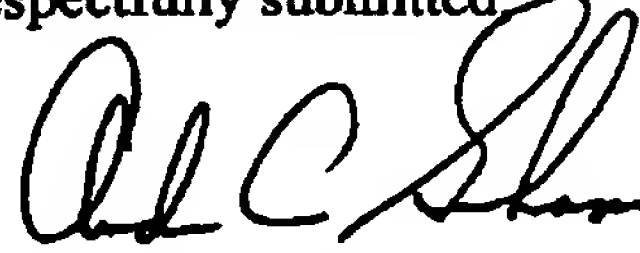
In summary, claims 9-36 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

PATENT

<b>CERTIFICATE OF MAILING OR TRANSMISSION</b>	
I hereby certify that, on the date shown below, this correspondence is being	
<input type="checkbox"/>	deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
<input checked="" type="checkbox"/>	facsimile transmitted to the US Patent and Trademark Office.
 Andrew C. Graham	7/30/04 Date

EXPRESS MAIL LABEL: \_\_\_\_\_

Respectfully submitted



Andrew C. Graham, Reg. No. 36,531  
Attorney for Applicant(s)  
(512) 338-6313  
(512) 338-6301 (fax)